S/N Unknown PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Thomas A. Figura	Examiner: Unknown
Serial No.:	10/004,656	Group Art Unit: 2813
Filed:	December 4, 2001	Docket: 303.645US2
Title:	METHOD AND STRUCTURE FOR IMPROVED ALIGNMENT TOLERANCE IN MULTIPLE, SINGULARIZED PLUGS	

SUPPLEMENTARY PRELIMINARY AMENDMENT

Commissioner for Patents
Washington, D.C. 20231

When the above-identified patent application is taken up for consideration, please amend the application as follows:

IN THE CLAIMS

Please substitute the claim set in the appendix entitled Clean Version of Pending Claims for the previously pending claim set. The substitute claim set is intended to reflect amendments of previously pending claims 11-22 and 29-34. The specific amendments to the individual claims are detailed in the following marked up set of claims.

11.(Amended) [A memory device] An integrated circuit, comprising:

multiple insulated wordlines having top surfaces, wherein the insulated wordlines are spaced apart from one another and formed on a substrate;

a bitline plug located between an adjacent pair of the insulated wordlines, the bitline plug having a top surface beneath the top surfaces of the insulated wordlines;

a pair of storage node plugs located on the opposite side of the adjacent pair of insulated wordlines from the bitline plug, wherein the pair of storage node plugs each have a top surface above the top surfaces of the insulated wordlines and are formed over portions of the adjacent wordlines;

a buried bitline coupled to the bitline plug; and